Application No.: 10/735,523

Response to Feb. 23, 2005 Office Action

PATENT Page 2 of 28

Amendments to the Specification

Please replace paragraph [0007] with the following amended paragraph:

[0007] Communication systems which transmit and receive signals often employ one or more mixing circuits to translate signals at [[a]] one frequency to another frequency. As known to the practitioner, the mixing circuits usually include two input ports for receiving two signals, typically identified as RF and LO signals, and an output port for providing a signal at the mixing product of the two input signals. As is well known, the mixing product of the two signals, typically referred to as the IF signal, may be expressed as:

 $IF = IMf_{RF} \pm Nf_{LO}I$

Please replace paragraph [0011] with the following amended paragraph:

[0011] Fig. 1B illustrates the doubly balanced mixer of Fig. 1A as a Gilbert cell multiplier or mixer circuit known in the art. The mixer circuit includes two cross-coupled differential transistor pairs 122 whose base terminals are coupled to the LO source 125, collector terminals are coupled to the IF loads 130, and emitter terminals are coupled to buffer transistors 117. Responsive to the differential RF signal applied at terminals 110a and 110b, a voltage difference is established across resistor 115, resulting in the corresponding modulation of the quiescently-supplied current driving the transistor pairs 122 that comprise the mixer core. Those skilled in the art will appreciate that the illustrated mixer circuit is only exemplary, and numerous variations of the circuit are also widely used.

Application No.: 10/735,523 Response to Feb. 23, 2005 Office Action PATENT Page 3 of 28

Please replace paragraph [0029] with the following amended paragraph:

[0029] Fig. 3A illustrates a simplified switch diagram of a mixer circuit 300 in accordance with one embodiment of the present invention. The mixer circuit 300 includes a mixer core 320 and a mode select circuit 340. The mixer core 320 includes two input switches 324 and 328, each switch having an input 324a, 328a, and two outputs 324b, 324c, and 328b, 328c, respectively. Switches are depicted to convey the component's general function, and those skilled in the art will readily appreciate that each may be realized using [[an]] a variety of circuit elements, including transistors (BJT and FET types), diodes, and the like. Accordingly, as used herein, the term "switch" or "switches" shall denote any of these circuit elements, or equivalents thereof.

Please replace paragraph [0031] with the following amended paragraph:

The first and second switches 324 and 328 are further configured to receive a switching signal 125, which operates to switch the first and second switches between their respective output states at a second frequency f₂, as will be further described below. In [[a]] the particular embodiment shown, the first and second switches 324 and 328 are configured such that both, upon receiving the switching signal 125, switch to the opposite states (i.e., one to its first output, and the other to its second output). In such an embodiment, the switching signal 125 may be supplied in antiphase to configure the first and second switches in opposite output states.

Please replace paragraph [0039] with the following amended paragraph:

[0039] In a specific embodiment of the mixer circuit 380, transistors Q1-Q8 are npn bipolar transistors 20 um x 0.4 um, IF loads 365a and 365b are 200 ohms, resistor 115 is 200 ohms, the first frequency f₁ operates at 950-2150 MHz, the second

Application No.: 10/735,523 Response to Feb. 23, 2005 Office Action PATENT Page 4 of 28

frequency signal f₂ operates at 3100 MHz, and the mode select signal 350 is 500 mV DC. The circuit's supply V_{CC} operates at +6 VDC. Further specifically, the illustrated components are integrally formed using a 0.35 um Bi-CMOSC photolithographic process. Skilled practitioners will appreciate that [[that]] the circuit 380 can be alternatively realized using various modifications, e.g., pnp-type bipolar transistors, n or p-type filed effect transistors, or other components such as diodes, and the like

Please replace paragraph [0043] with the following amended paragraph:

The mixer circuits 380₁₋₃ are supplied respective mode select signals 350₁₋₃ to configure each corresponding mixer circuit to their its desired output. In the shown embodiment, the first mixer circuit 380₁ is supplied a "bypass" mode signal 350₁, resulting in the (differential) output at the first signal frequency f₁. The second mixer circuit 380₂ is supplied a "mix" mode signal 350₂, resulting in the output of the mixing product described above. Similarly, the third mixer circuit 380₃ receives the first and second frequency signals f₁, f₂, and the "mix" mode signal 350₃, resulting in the mixing mode of operation. Preferably, the first and second switches of each mixer circuit 380₁₋₃ continue[[s]] to switch at the second frequency f₂ regardless of whether the supplied control signal 350₁₋₃ sets the mixer circuit to a bypass mode or mixing mode. Additionally, the mixer circuit's coupling to the IF loads 365a and 365b (or to a single IF load coupled between differential nodes 130a and 130b) is maintained during and switching between the bypass and mixing modes.